Remarks

Thorough examination by the Examiner is noted and appreciated.

The specification has been amended in accordance with Examiners objection to the use of metal nitride and metal carbide to describe e.g., silicon nitride, and silicon carbide. Applicants have eliminated the use of the term **metal**, thereby reciting carbides and nitrides to correctly include disclosed materials e.g., silicon nitride, silicon oxynitride, silicon carbide, and titanium nitride.

In addition, the specification has been amended to correct some grammatical errors.

The claims have been amended to clarify Applicants disclosed and claimed invention and new claims added. Support for the amended claims is found in the original claims and/or Specification. No new matter has been entered. For example support for new limitations in claim 12 is found in the Specification at line 13, page 14:

"Plasma etching is then carried out to etch through the first etching stop layer 24A to form an opening 30, for example a via opening, **in closed communication with conductive area 22B** as shown in Figure 2B after stripping the photoresist layer 28A."

and at page 12, beginning at line 4:

"Overlying the first etching stop layer 24A **is an inter-metal dielectric (IMD) layer 26 (insulating layer)** for subsequently etching a semiconductor feature, for example, a via opening"

Support for new claims 21 and 22 is found in the Specification at page 12, beginning at line 4:

"Overlying the first etching stop layer 24A is an inter-metal dielectric (IMD) layer 26 (insulating layer) for subsequently etching a semiconductor feature, for example, a via opening, the IMD layer being formed of, for example, silicon dioxide, or a low-k doped silicon dioxide. Typically, the dielectric constant of the low-k material is less than about 3.0 to minimize electrical parasitic capacitive effects. It will be appreciated that other low-k materials may be used and that the method according to the present invention is likewise applicable to those materials, particularly if they are porous materials. Additional exemplary low-k inorganic materials include, for example, dope and undoped porous oxides, xerogels, or SOG (spin-on glass). Exemplary low-k organic materials include, for example, polysilsequioxane, parylene, polyimide, benzocyclobutene amorphous Teflon, and spin-on polymer (SOP)."

Support for new claim 23 is found in the Specification at page 16, beginning at line 14:

"Exemplary polymers include, for example, include methyl methacrylate, polyolefins, polyacetals, polycarbonates, polypropylenes and polyimides. Alternatively, the via plug 34 may be formed of an oxide, for example, the same material as the IMD layer 26 and deposited by a spin-on or CVD process."

Claim Rejections under 35 USC 112

1. Claims 6 and 16 stand rejected under 35 USC 112, second paragraph as being indefinite for failing to particularly and distinctly claim the subject matter which Applicants regard as their invention.

Claims 6 and 16 have been amended to overcome Examiners rejection by eliminating the use of the word "metal", using the terms of art "carbide" and "nitride" thereby including disclosed carbides such as silicon carbide as well as nitrides such as silicon nitride, silicon oxynitride, and titanium nitride.

Claim Rejections under 35 USC 102

2. Claims 1-2, and 12 stand rejected under 35 USC 102(e) as being anticipated by Zhou et al. (US Pat. 6,358,842).

Zhou et al. disclose and teach a method for forming a protective passivation layer on via openings sidewalls using a sulfur containing gas to strip photoresist following etching of the via. Zhou et al. teach a method whereby the via is etched in dielectric insulating layers comprising a lower dielectric insulating layer separated by an etch stop layer from an upper dielectric insulating layer for forming a single or dual damascene, (see Abstract, Figures 8, 13).

Significantly, Zhou et al. teach **simultaneously** forming the sidewall passivation layer during stripping of the photoresist (col 6, lines 15-25). The sulfur containing sidewall passivation layer is taught to prevent etching of the via side walls in a subsequent etching step to etch through an underlying passivation layer to expose a metal (e.g., copper) interconnect) (see e.g., col 6, lines 25-34).

In contrast, Applicants disclose and claim in amended claim 1:

"A dual damascene formation method for reducing a faceted etching profile at a trench/via interface comprising the steps of:

providing a substrate comprising a silicon oxide containing dielectric insulating layer;

providing a first patterned photoresist layer exposing an uppermost layer of the substrate for plasma etching a first opening;

plasma etching through a first thickness portion of the dielectric insulating layer to form the first opening;

removing the first patterned photoresist layer;

blanket depositing an etching stop liner to line the sidewalls of the first opening;

at least partially filling the first opening with a plug of resinous material;

photolithographically patterning a second photoresist layer for etching a second opening at least partially overlying and encompassing the first opening; and,

plasma etching through a second thickness portion of the dielectric insulating layer to form the second opening."

Nowhere do Zhou et al. disclose the step of forming the liner following removal of the photoresist or disclose at least partially filling the first opening with a plug of resinous material prior to a trench patterning and etching step.

Zhou et al. is clearly insufficient to anticipate Applicants disclosed and claimed invention.

Claim Rejections under 35 USC 103

3. Claims 3-7, 13 stand rejected under 35 USC 103(a) as being unpatentable Zhou et al., above, in view of Zhao (US 6,329,290).

Applicants reiterate the comments made above with respect to Zhou et al.

Zhao, on the other hand disclose a method for forming a dual damascene structure where a liner is deposited following removing a first patterned photoresist layer and prior to forming an overlying trench opening (see Abstract; col 2, lines 35-50).

Zhao teaches that following formation of the overlying trench, an etching process to remove the bottom portion of the liner results in rounding off of the liner layer (col 8, lines 15-26). Zhao discloses alternate methods for forming a dual damascene including where an etch stop layer separates and upper and lower dielectric insulating layer and where the dual damascene (via and trench portions) are formed in a single dielectric insulating layer (see e.g., col 5, lines 15-22).

Zhao therefore, teaches away from Applicants disclosed and claimed invention. Zhao discloses using **either** two separate dielectric insulating layers separated by an etch stop layer **or** a single dielectric insulating layer. Zhao does not recognize or discuss the problem that Applicants have recognized and solved by their claimed invention: "A dual damascene formation method for reducing a faceted etching profile at a trench/via interface". Zhao nowhere discuss a problem of a faceted etching profile at a via/trench interface or suggest a solution thereto.

Moreover, Zhao does not disclose or suggest forming a plug of resinous material to at least partially fill the first opening prior to patterning and etching an overlying trench. Moreover, there is no apparent motivation for combining Zhao and Zhou et al. The formation of a sulfonated passivation layer

simultaneously with the stripping of the via patterned photoresist in the method of Zhou et al. is incompatible with the principal of operation of depositing a conformal dielectric liner layer following removal of the resist in the method of Zhao. Moreover, it is not clear that the sulfur containing (sulfonated) layer of Zhou et al. could be deposited following the removal of the photoresist layer as in the disclosed dielectric layers e.g., silicon nitride of Zhao for the purpose of reducing a via opening width.

Nevertheless, assuming *arguendo* proper motivation for combining Zhou et al. and Zhao, such combination does not produce Applicants disclosed and claimed invention, but rather teaches away therefrom.

"A prior art reference must be considered in its entirety, i.e., as a whole including portions that would lead away from the claimed invention." *W.L. Gore & Associates, Inc., Garlock, Inc., 721 F.2d, 1540, 220 USPQ 303 (Fed Cir. 1983), cert denied, 469 U.S. 851 (1984).*

"If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification." *In re Gordon, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).*

4. Claims 8-11 and 18-20 stand rejected under 35 USC 103(a) as being unpatentable Zhou et al., above, in view of Hussein et al. (US 6,406,995).

Hussein et al. teaches at least partially filling a via opening with a plug of resinous material (sacrificial material) **in order to protect an underlying etch stop layer** prior to forming an overlying trench portion of a dual damascene (see e.g., Abstract, col 5, lines 28-36). There is no suggestion anywhere in the teachings of Hussein et al, **that in addition to or in place of the plug of material**, a liner material should be deposited in the via opening. Since plug of Hussein et al. is for the purpose of protecting the underlying etch stop covering a metal interconnect in the trench etching step there is no apparent need for or suggestion for depositing a liner material as Applicants have claimed.

On the other hand, in the method of Zhou et al., there is no suggestion that a dielectric liner material is needed over the etch stop layer at the bottom of the via, or that the etch stop layer (barrier layer) needs protection during the trench etching step. Moreover, one of the key points of the method of Zhou et al., is that the sulfur containing passivation layer can be accomplished while removing the photoresist layer thereby not

requiring any additional steps (see col 9, lines 1-6) e.g., forming a plug of filling material as in Hussein et al., thereby teaching away from the combination of Zhou et al. and Hussein et al.

Examiner is apparently engaged in impermissible hindsight reasoning, using Applicants disclosed invention as a roadmap to combine elements of the prior art absent any teaching or suggestion to do so other than Applicants disclosure.

Nevertheless, even assuming *arguendo* proper motive for combination, such combination does not produce Applicants claimed invention, particularly as claimed by Applicants in claim 12, where the via opening is formed in closed communication with an underlying conductive area prior to forming the liner layer and via plug.

"First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. **The teaching or suggestion to make the**

claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

Applicants point out that "we do not pick and choose among the individual elements of assorted prior art references to recreate the claimed invention, but rather we look for some teaching or suggestion in the references to support their use in a particular claimed combination" *Symbol Technologies, Inc. v. Opticon, Inc., 935 F.2d 1569, 19 USPQ2d 1241 (Fed. Cir. 1991).*

The claims have been amended and new claims added to clarify Applicants disclosed and claimed invention. A favorable consideration of Applicants' claims is respectfully requested.

Based on the foregoing, Applicants respectfully submit that the Claims are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited. In the event that the present invention as claimed is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his

Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

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